	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif	Inventor▵
1	☒	☐	US 5239271 A	19930824	9	Microwave synthesizer	327/105			Ben-Efraim, Gideon
2	☒	☐	US 6115586 A	20000905	12	Multiple loop synthesizer for radio frequency signals, has three phase locked loops with single sideband mixer between second and third phase locked loops				BEZZAM, I et al.
3	☒	☐	US 6115586 A	20000905	12	Multiple loop radio frequency synthesizer	455/112	327/105; 327/113; 332/117; 455/113; 455/118; 455/126; 455/76		Bezzam, Ignatius et al.
4	☒	☐	US 6356810 B1	20020312	32	Programmable frequency reference for a signal synthesizer	700/298	331/177R; 331/18		Bradley, Donald A.
5	☒	☐	US 6191657 B1	20010220	7	Frequency synthesizer with a phase-locked loop with multiple fractional division	331/1A	331/25		Brunet, Elie et al.
6	☒	☐	US 5508659 A	19960416	10	Single loop frequency synthesizer with direct digital synthesis	331/16	327/105; 327/156; 331/14; 331/17; 331/18; 455/260		Brunet, Elie et al.
7	☒	☐	US 3805181 A	19740416	8	FREQUENCY SYNTHESIZER WITH MULTIPLE CONTROL LOOPS	331/2	331/11; 331/14; 331/19		Charbonnier, Roger
8	☒	☐	US 4862109 A	19890829	6	Processor controlled phase locked loop multi-band frequency synthesizer	331/16	331/25		Cowley, Nicholas P.
9	☒	☐	US 6005443 A	19991221	11	Phase locked loop frequency synthesizer for multi-band application	331/14	331/16; 331/17; 331/25		Damgaard, Morten et al.
10	☒	☐	US 4912432 A	19900327	12	Plural feedback loop digital frequency synthesizer	331/2	331/25; 331/31		Galani, Zvi et al.
11	☒	☐	US 5777521 A	19980707	13	Parallel accumulator fractional-n frequency synthesizer	331/16	331/25; 377/48		Gillig, Steven F. et al.

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif	Inventor△
12	☒	☐	US 5028887 A	19910702	15	Direct digital synthesizer driven phase lock loop frequency synthesizer with hard limiter	331/18	327/107; 331/25; 708/276		Gilmore, Robert P.
13	☒	☐	US 4965533 A	19901023	11	Direct digital synthesizer driven phase lock loop frequency synthesizer	331/18	331/25		Gilmore, Robert P.
14	☒	☐	US 5055803 A	19911008	9	Parameter tolerant PLL synthesizer	331/17	331/1A; 331/16; 331/25		Hietala, Alexander W.
15	☒	☐	US 6172937 B1	20010109	11	Multiple synthesizer based timing signal generation scheme	365/233	365/193		Ilkbahar, Alper et al.
16	☒	☐	US 6373344 B1	20020416	18	High performance dual-YTO microwave synthesizer	331/96	331/175; 331/34		Mar, Wing J.
17	☒	☐	US 5128633 A	19920707	10	Multi-loop synthesizer	331/2	327/105; 331/25		Martin, Frederick L. et al.
18	☒	☐	US 6028460 A	20000222	11	Hybrid analog-digital phase lock loop multi-frequency synthesizer	327/105	327/156; 327/159; 331/11		McCollum, Robert L. et al.
19	☒	☐	US 6229494 B1	20010508	20	Radiation synthesizer systems and methods	343/741	343/701		Merenda, Joseph T.
20	☒	☐	US 5365202 A	19941115		PLL frequency synthesizer using plural phase comparisons	331/12	331/17; 331/25		Mori, Kazuhiro
21	☒	☐	US 4839603 A	19890613		Multiple-loop microwave frequency synthesizer using two phase lockloops	327/105	327/113; 331/2; 331/22		Mower, Vaughn L. et al.
22	☒	☐	US 6216254 B1	20010410		Integrated circuit design using a frequency synthesizer that automatically ensures testability	716/5	324/76.39; 324/76.41; 324/76.53; 326/16; 326/39; 713/500; 714/733; 716/16; 716/2; 716/4; 716/7		Pesce, Michael S. et al.

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Classif	Inventor▵
23	☒	☐	US 4458329 A	19840703	6	Frequency synthesizer including a fractional multiplier	708/845	327/105; 331/2; 708/103; 708/835		Remy, Joel
24	☒	☐	US 4225830 A	19800930		Plural phase locked loop frequency synthesizer	331/2	331/25		Remy, Joel
25	☒	☐	US 20020140512 A1	20021003		Polyphase noise-shaping fractional-N frequency synthesizer	331/11	331/17; 331/18; 331/25		Stockton, David
26	☒	☐	US 6509800 B2	20030121		Polyphase noise-shaping fractional-N frequency synthesizer	331/11	327/115; 331/10		Stockton, David
27	☒	☐	US 3959737 A	19760525		Frequency synthesizer having fractional frequency divider in phase-locked loop	331/1A	331/11; 331/17; 331/25; 377/48		Tanis, William J.
28	☒	☐	US 5258724 A	19931102		Frequency synthesizer	331/1A	327/105; 327/28; 331/10; 331/25		Tanis, William J. et al.
29	☒	☐	US 5146187 A	19920908		Synthesizer loop filter for scanning receivers	331/17	331/16; 331/25; 333/174		Vandegraaf, Johannes J.
30	☒	☐	US 5146186 A	19920908		Programmable-step, high-resolution frequency synthesizer which substantially eliminates spurious frequencies without adversely affecting phase noise	331/16	331/11; 331/18; 331/19; 455/260		Vella, Paul L.
31	☒	☐	US 4320357 A	19820316		VHF-FM Frequency synthesizer	331/16	331/179; 331/18; 331/25; 332/127		Wulfsberg, Paul G. et al.
32	☒	☐	US 5332978 A	19940726	15	Frequency synthesizer	331/2	331/11; 331/14; 331/25		Yabuki, Hiroyuki et al.

US006373344B1

(12) **United States Patent**
Mar

(10) **Patent No.: US 6,373,344 B1**
(45) **Date of Patent: Apr. 16, 2002**

(54) **HIGH PERFORMANCE DUAL-YTO MICROWAVE SYNTHESIZER**

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(73) Assignee: **Agilent Technologies, Inc.**, Palo Alto, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/733,877**

(22) Filed: **Dec. 8, 2000**

(51) **Int. Cl.**[7] **H03B 5/18**

(52) **U.S. Cl.** **331/96**; 331/34; 331/175

(58) **Field of Search** ..... 331/2, 10, 47, 331/34, 96, 175, 177 R

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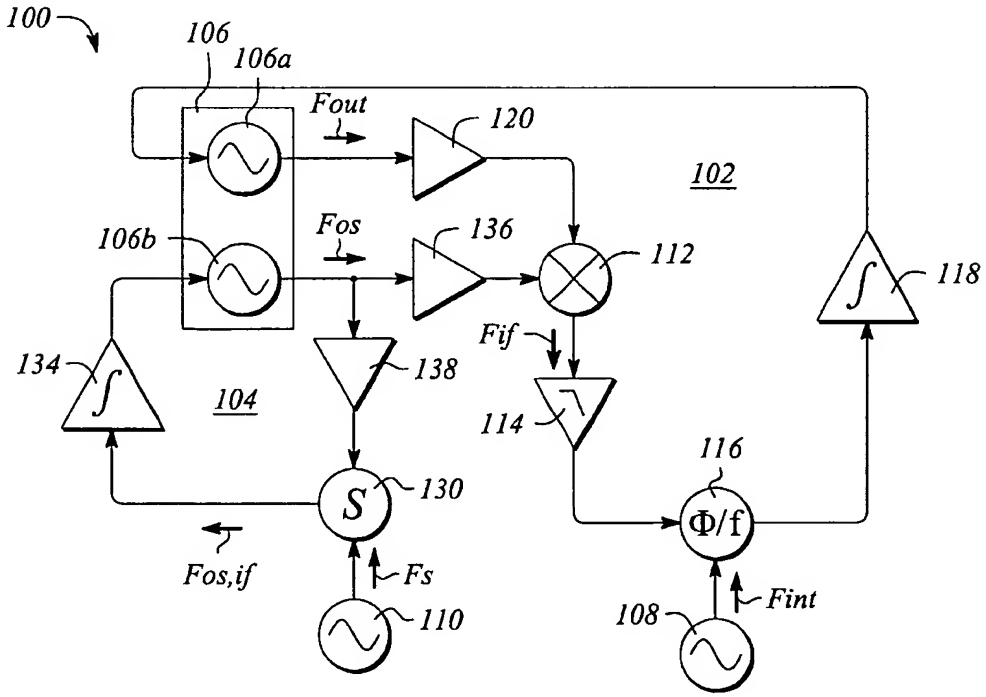
Primary Examiner—David Mis

(57) **ABSTRACT**

A microwave synthesizer apparatus features very low phase noise, fine frequency resolution and wide tuning range coverage. The microwave synthesizer apparatus utilizes a fundamental offset source in an offset phase lock loop (PLL) to translate an output signal Fout to a lower IF signal Fif for locking to a low frequency interpolation signal Fint. The use of the fundamental offset source instead of the conventional multiple frequency offset signal from a comb generator or sampler results in superior phase noise and spurious performance. The synthesizer comprises a main signal loop having a main loop VCO that produces an output signal Fout and an offset signal loop having an offset VCO that produces an output signal Fos. The signals Fos and Fout are mixed in the main loop to control the frequency of the signal Fout. The main loop VCO and the offset loop VCO preferably are YIG-tuned Oscillators (YTOs) that share a main coil. Moreover, the main YTO and the offset YTO preferably have a common housing and further, each of the main YTO and the offset YTO has a separate FM coil. The use of a dual YTO in the microwave synthesizer apparatus minimizes overall cost and power consumption of the synthesizer by combining the dual YTO in the single package. In one embodiment, the microwave synthesizer further comprises a mode selection feature that selects between operation of the synthesizer in an offset or dual loop mode and a variable divider or single loop mode. In another embodiment, the microwave synthesizer further comprises a selectable frequency divider that produces the output signal Fos with a smaller frequency step size.

26 Claims, 6 Drawing Sheets



US005152005A

United States Patent [19]

Bickley

[11] Patent Number: 5,152,005

[45] Date of Patent: Sep. 29, 1992

[54] HIGH RESOLUTION FREQUENCY SYNTHESIS

[75] Inventor: Robert H. Bickley, Scottsdale, Ariz.

[73] Assignee: Motorola, Inc., Schaumburg, Ill.

[21] Appl. No.: 774,173

[22] Filed: Oct. 15, 1991

Related U.S. Application Data

[63] Continuation of Ser. No. 468,440, Jan. 22, 1990, abandoned.

[51] Int. Cl.[5] H04B 1/40; H04B 17/02; H03L 7/00

[52] U.S. Cl. 455/76; 455/165.1; 455/182.1; 455/183.1; 455/192.1; 455/260; 331/2; 331/25

[58] Field of Search 455/75-76, 455/165, 182, 183, 192, 260; 328/14; 307/529; 331/2, 25

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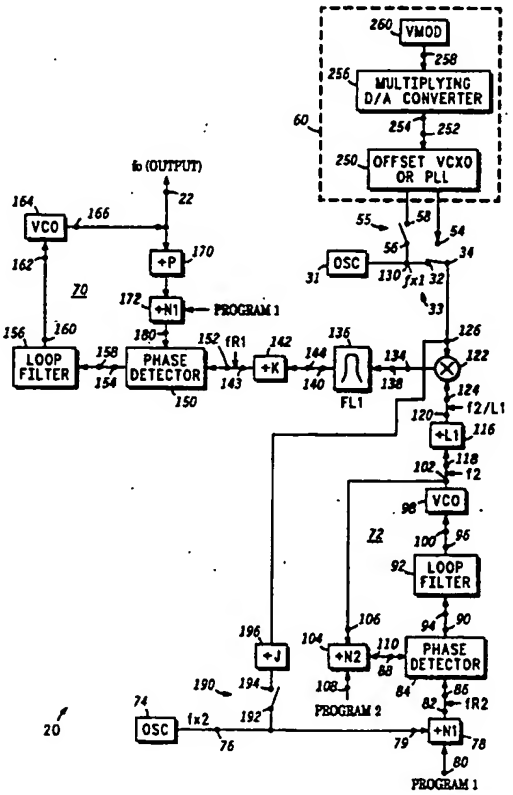
Primary Examiner—Reinhard J. Eisenzopf
Assistant Examiner—Andrew Faile
Attorney, Agent, or Firm—Robert M. Handy; Maurice J. Jones

[57] ABSTRACT

The synthesizer includes an output PLL having a divide-by-N1 divider in its feedback loop. The output PLL is couples through frequency offset circuitry to receive a reference signal from a driver PLL having a divide-by-N2 divider in its feedback loop. Another divide-by-N1 divider coupled a reference oscillator to the driver PLL. The reference oscillator provides another reference signal. As a result, the setting for N1 controls the course frequency tuning and the setting for N2 controls the fine frequency tuning of the synthesizer which provides any one of a plurality of selectable predetermined output frequencies. The adjacent selectable frequencies are closer together than the frequencies of the reference signals. The synthesizer has a simple configuration and provides a high degree of output frequency resolution, fast acquisition and low noise.

37 Claims, 3 Drawing Sheets



L Number	Hits	Search Text	DB	Time stamp
1	55	(@ad<=20011021) and (multiple or multi$3) near3 loop$1 near3 synthesizer$1	USPAT; US-PGPUB; DERWENT	2004/04/01 15:04
2	9	(((@ad<=20011021) and (multiple or multi$3) near3 loop$1 near3 synthesizer$1) and fine and coarse	USPAT; US-PGPUB; DERWENT	2004/04/01 15:04
3	6	((((@ad<=20011021) and (multiple or multi$3) near3 loop$1 near3 synthesizer$1) and fine and coarse) and mixer	USPAT; US-PGPUB; DERWENT	2004/04/01 15:04